Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**.106”**



**.106”**

**Top Material: Al**

**Backside Material: Ag**

**Bond Pad Size: B = .025 x .033”**

**E = .030 x .036”**

**Backside Potential: COLLECTOR**

**Mask Ref: CP235**

**APPROVED BY: DK DIE SIZE .106” X .106” DATE: 10/13/21**

**MFG: CENTRAL SEMI THICKNESS .012” P/N: 2N3715**

**DG 10.1.2**

#### Rev B, 7/1